In the Specification

Please replace the following paragraphs of the Specification:

[0002] Digital electronic signals are used to communicate digital information. This communication may be from one ~~on~~ device to another, one integrated circuit (or chip) to another, or within an integrated circuit itself. In many of these applications, the difference between the ~~a~~ voltage level that denotes a "high" (or logical "1") and the voltage level that denotes a "low" (or logical "0") has been getting smaller. Designers have chosen these smaller differentials for reasons that include: lower power supply voltages, increasing switching speed, lowering power consumption, and the use of standard bus interfaces that have defined smaller voltage differentials.

[0011] Also note that, as shown in FIG. 1, it takes less time for the input signal 102 to cross the dynamically controlled reference voltage 104 than it does the static reference voltage 106. This is shown as Δt ~~At~~ in FIG. 1. Since the dynamically controlled reference voltage 104 has moved closer to the input signal 102 voltage than the static reference voltage 106 (which does not move) near the end of each bit-time, an input signal 102 transition with a non-infinite slope crosses the dynamically controlled reference voltage 104 level sooner than it crosses the static reference voltage 106 level. This illustrates that an input signal 102 transition can be detected faster with the dynamically controlled reference voltage 104 than it can be detected with a static reference voltage 106.

[0013] In a step 214, the system waits for a transition. Since it was determined in step 202 that the current state of the input signal was at a high voltage, or because flow ~~low~~ to step 214 came from step 206 just after a low-to-high transition, the transition in step 214 would be a high-to-low transition. After this transition, flow proceeds to step 216. In a step 216, the reference voltage is ramped-up from its present voltage to a higher voltage. Flow then proceeds to step 204.

[0014] FIG. 3 is a schematic diagram illustrating a circuit that dynamically controls a reference voltage. In FIG. 3, a resistive ladder network 302 provides numerous different voltages to an analog multiplexer (MUX) 304 via analog signal lines 310. One of these numerous different voltages is selected, according to the digital values on counter outputs 312, by MUX 304, which ~~and~~ outputs a dynamically controlled reference voltage, VREF. Resistive ladder 302 may divide down the supply voltages or another reference voltage supplied to it to generate these different voltages.

[0016] Signal OUT also controls the direction of saturating binary counter 306. By saturating binary counter it is meant that the counter outputs 312 of counter 306 do ~~does~~ not "rollover" from their ~~its~~ lowest value to their ~~is~~ highest value when counting down and do ~~does~~ not "rollover" from their ~~its~~ highest value to their ~~its~~ lowest value when counting up. Instead, the counter outputs 312 reach these values and hold them until the direction control (UP/DOWN) changes state.